REMARKS

Claims 13-18 remain pending in the application, claims 1-12 being withdrawn from consideration by the Examiner and subsequently canceled herein.

Claims 13, 14, 16, 17 over Nonaka; and claims 15, 18 over Nonaka and Wolf

Claims 13, 14, 16 and 17 were rejected under 35 U.S.C. §102(e) as allegedly being anticipated by U.S. Patent No. 6,781,238 to Nonaka ("Nonaka"); and claims 15 and 18 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Nonaka in view of Silicon Processing for the VLSI Era, v. 2, by Wolf ("Wolf"). The Applicants respectfully traverse the rejections.

Claims 13-18 recite **over-routing SIGNAL bearing metal lines** over a first plurality of parallel traces routed to power and a second plurality of parallel traces routed to ground, wherein the pattern provides metal fill as a first purposeful function, and as a second purposeful function provides capacitance across a power supply, and electro-magnetic shielding to protect an analog circuit therebelow from the **over-routed SIGNAL bearing metal lines**.

The Examiner cites Nonaka, in particular col. 9, lines 16-25; and col. 10, lines 6-17. The cited embodiment of Nonaka teaches construction of a bypass capacitor in the PAD AREA **13** at the TOP of the integrated circuit (IC). See, for example, Figs. 7A,7B and 7C wherein the GND wire 27b and the VDD wire 26B are both formed at the TOP of the IC.

The present invention importantly provides electro-magnetic shielding to protect an analog circuit below the fill pattern from **OVER-ROUTED SIGNAL BEARING METAL LINES** above the fill pattern, as claimed by claims 13-18. As disclosed in the specification, e.g., at page 7, lines 15-28, which reads:

> *The lines of interdigitated fingers **120**, **128** forming the cross-fill metal fill pattern are routed over the cell of an IC module, and thus shield underlying devices (e.g., sensitive analog devices) composing the module. This is particularly useful to shield underlying sensitive analog circuitry from signal lines routed*

> *above the layer(s) containing the cross-fill metal fill pattern. For instance, in one embodiment, metal signal lines were routed over an insulative layer formed over a cross-fill metal fill pattern layer, with a distance between the routed metal signal lines and the underlying cross-fill metal fill pattern of about 7200 angstroms. The cross-fill pattern provided a suitable electro-magnetic shielding function to shield underlying sensitive analog circuitry.*

Nonaka fails to disclose or teach the important aspect of providing electro-magnetic shielding to protect an analog circuit below the fill pattern from **OVER-ROUTED SIGNAL BEARING METAL LINES** above the fill pattern, as claimed by claims 13-18

With respect to claims 15 and 18, the Examiner further cites Wolf as allegedly teaching provision of an analog circuit, and alleges that "Nonaka would look to one such as Wolf for interfacing with analog structures because Wolf discloses providing an analog circuit with several types of integrated circuits" (Office Action at 4) Even if this were the case, Wolf fails to disclose use of a capacitive fill pattern above the analog circuit, much less signal bearing metal lines routed ABOVE such a capacitive fill pattern as claimed by claims 13-18.

For these and other reasons, claims 13-18 are patentable over the prior art of record. It is therefore respectfully requested that the rejections be withdrawn.

Conclusion

All objections and rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,
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